CLAIMS

What is claimed is:

1. A method for forming a gate stack having improved electrical properties in a gate structure forming process comprising the steps of:

providing a semiconductor substrate;

forming a metal oxide layer over an exposed portion of the semiconductor substrate; and,

forming a layer of ELECTRODE over the metal oxide layer in a nitrogen containing ambient.

2. The method of claim 1, wherein an interfacial layer having a thickness of less than about 15 Angstroms is formed over the silicon substrate prior to forming the metal oxide layer the interfacial layer comprising at least one of silicon oxide, silicon oxynitride, silicon nitride, and aluminum oxide.

3. The method of claim 2, wherein the interfacial layer is formed having a thickness less than about 10 Angstroms.

4. The method of claim 2 wherein the interfacial layer comprises a native oxide formed over the silicon substrate following a cleaning process.

5. The method of claim 1, wherein the metal oxide layer comprises a dielectric constant of greater than about 20.

6. The method of claim 1, wherein the metal oxide is formed having a thickness of about 20 Angstroms to about 100 Angstroms.

7. The method of claim 1, wherein the gate stack including the metal oxide layer is formed to have a dielectric thickness equivalent to a silicon dioxide dielectric thickness of less than about 20 Angstroms.

8. The method of claim 6, wherein the metal oxide is selected from the group consisting of tantalum oxides, titanium oxides, zirconium oxides, hafnium oxides, and yttrium oxides.

9. The method of claim 8, wherein the metal oxide is formed from one of a metal-organic CVD method and an atomic layer deposition (ALD) method.

10. The method of claim 9, wherein an ozone containing oxidation process is carried out to treat the metal oxide layer following the formation of the metal oxide layer.

11. The method of claim 1, wherein a layer comprising aluminum oxide is formed over the metal oxide layer prior to forming the polysilicon layer.

12. The method of claim 11, wherein the aluminum oxide layer is formed having a thickness of about 5 Angstroms to about 15 Angstroms.

13. A method for forming a high dielectric constant gate structure comprising the steps of:

providing a silicon-containing substrate comprising exposed surface portions;

forming an interfacial layer over the exposed surface portions having a thickness of less than about 10 Angstroms;

forming a high dielectric constant metal oxide layer over the interfacial layer having a dielectric constant of greater than about 10;

forming a barrier layer over the high dielectric constant metal oxide layer;

forming an electrode layer over the barrier layer; and

etching according to an etching pattern through a thickness of the electrode layer, barrier layer, high dielectric constant material layer, and the interfacial layer to form a high dielectric constant gate structure.

14. The method of claim 13, wherein the barrier layer comprises aluminum oxide for preventing chemical interaction with the electrode layer comprising polysilicon.

15. The method of claim 14, wherein the barrier layer is formed having a thickness of about 5 Angstroms to about 15 Angstroms.

16. The method of claim 13, wherein the interfacial layer is selected from the group consisting of silicon oxide, silicon oxynitride, silicon nitride, and aluminum oxide.

17. The method of claim 13, wherein the high dielectric constant metal oxide layer is formed having a thickness of about 20 Angstroms to about 100 Angstroms.

18. The method of claim 13, wherein the high dielectric constant metal oxide layer is selected from the group consisting of tantalum oxides, titanium oxides, zirconium oxides, hafnium oxides, and yttrium oxides.

19. The method of claim 13, wherein the high dielectric constant metal oxide layer comprises a dielectric constant of greater than about 20.

20. The method of claim 13, wherein the high dielectric metal oxide layer and the barrier layer are formed from one of a metal-organic CVD process and an atomic layer deposition (ALD) process.

21. The method of claim 13, wherein the interfacial layer, the high dielectric constant metal oxide layer, and the barrier layer comprise a gate stack having a dielectric constant value about equal to a silicon dioxide layer thickness of about 10 to about 20 Angstroms.

22. The method of claim 13, further comprising forming a layer of polysilicon over the high dielectric constant metal oxide layer according to a CVD process carried out between about 100 milliTorr and about 760 Torr.

23. The method of claim 22 wherein the CVD process comprises a silane gas precursor and at least one of a nitrogen and hydrogen carrier gas.

24. An improved high dielectric constant gate structure comprising:

an interfacial layer disposed over a silicon-containing substrate having a thickness of less than about 10 Angstroms;

a high dielectric constant metal oxide layer disposed over the interfacial layer having a dielectric constant of greater than about 10;

a barrier layer disposed over the high dielectric constant metal oxide layer; and,

an electrode layer disposed over the barrier layer.

25. The high dielectric constant gate structure of claim 24, wherein the barrier layer comprises aluminum oxide.

26. The high dielectric constant gate structure of claim 25, wherein the barrier layer is formed having a thickness of about 5 Angstroms to about 15 Angstroms.

27. The high dielectric constant gate structure of claim 24, wherein the interfacial layer is selected from the group consisting of silicon oxide, silicon oxynitride, silicon nitride, and aluminum oxide.

28. The high dielectric constant gate structure of claim 24, wherein the high dielectric constant metal oxide layer has a thickness of about 20 Angstroms to about 100 Angstroms.

29. The high dielectric constant gate structure of claim 24, wherein the high dielectric constant metal oxide layer is selected from the group consisting of tantalum oxides, titanium oxides, zirconium oxides, hafnium oxides, and yttrium oxides.

30. The high dielectric constant gate structure of claim 24, wherein the high dielectric constant metal oxide layer comprises a dielectric constant of greater than about 20.

31. The high dielectric constant gate structure of claim 24, wherein the high dielectric metal oxide layer and the barrier layer are formed from one of a metal-organic CVD process and an atomic layer deposition (ALD) process.

32. The high dielectric constant gate structure of claim 24, wherein the interfacial layer, the high dielectric constant metal oxide layer, and the barrier layer comprise a gate stack having a dielectric constant value about equal to a silicon dioxide layer thickness of about 10 to about 20 Angstroms.